Patent claims

1. A pulse generator circuit for generating an input signal for a flip flop circuit from a clock signal and from a data signal,

- comprising a clock pulse field effect transistor, at the gate terminal of which the clock signal can be applied and at the first source/drain terminal of which the input signal for a flip flop circuit can be provided;
- comprising a logic field effect transistor, at the gate terminal of which the data signal can be applied and the first source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor;
- comprising a feedback field effect transistor, at the gate terminal of which a feedback signal based on the clock signal can be applied, the first source/drain terminal of which is coupled to the second source/drain terminal of the logic field effect transistor and at the second source/drain terminal of which a first electrical reference potential can be applied;
- comprising a control unit for controlling the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor in such a manner that, for generating the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor for generating the flip flop signal.

2. The pulse generator circuit as claimed in claim 1, comprising an additional clock pulse field effect transistor, at the gate terminal of which the clock signal can be applied, at the first source/drain

terminal of which a second electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor.

3. The pulse generator circuit as claimed in claim 2, comprising an additional feedback field effect transistor, the gate terminal of which is coupled to the gate terminal of the feedback field effect transistor, at the first source/drain terminal of which the second electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor.

4. The pulse generator circuit as claimed in one of claims 1 to 3, comprising a bypass field effect transistor, the gate terminal of which is coupled to the flip flop circuit, at the first source/drain terminal of which the first electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor.

5. The pulse generator circuit as claimed in one of claims 1 to 3, comprising a bypass field effect transistor, the gate terminal of which is coupled to the flip flop circuit, the first source/drain terminal of which is coupled to the first source/drain terminal of the feedback field effect transistor, and the second source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor.

6. The pulse generator circuit as claimed in one of claims 1 to 5, in which the first electrical reference potential is an electrical ground potential and/or in which the second electrical reference potential is an

electrical supply potential.

7. The pulse generator circuit as claimed in one of claims 1 to 6, in which the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor are field effect transistors of the n-type of conduction.

8. The pulse generator circuit as claimed in one of claims 3 to 7, in which the additional clock pulse field effect transistor and the additional feedback field effect transistor are field effect transistors of the p-type of conduction.

9. The pulse generator circuit as claimed in one of claims 4 to 8, in which the bypass field effect transistor is a field effect transistor of the n-type of conduction.

10. The pulse generator circuit as claimed in one of claims 1 to 9, comprising a second signal path of additional field effect transistors which has the same circuit as the first signal path formed from the field effect transistors, which additional field effect transistors are interconnected for generating from the clock signal and from a complementary data signal which is complementary to the data signal a complementary input signal which is complementary to the input signal for the flip flop circuit.

11. The pulse generator circuit as claimed in claim 10, in which the first source/drain terminal of the additional clock pulse field effect transistor of the second signal path is coupled to the gate terminal of the additional feedback field effect transistor of

the first data path.

12. The pulse generator circuit as claimed in claim 10 or 11, in which the first source/drain terminal of the clock pulse field effect transistor of the first signal path is coupled to the gate terminal of the additional feedback field effect transistor of the second data path.

13. The pulse generator circuit as claimed in one of claims 1 to 12, in which the control unit is set up in such a manner that it applies the data signal to the gate terminal of the logic field effect transistor chronologically before the clock signal is switched for changing the clock pulse field effect transistor from a state with nonconducting channel region into a state with conducting channel region.

14. A circuit arrangement

- comprising a pulse generator circuit as claimed in one of claims 1 to 13;
- comprising a flip flop circuit which is interconnected with the pulse generator circuit in such a manner that the input signal which can be generated by the pulse generator circuit can be coupled into the flip flop circuit.

15. The circuit arrangement as claimed in claim 14, in which the flip flop circuit has storage field effect transistors for storing a storage signal based on the input signal and/or the complementary input signal.

16. The circuit arrangement as claimed in claim 15, in which the flip flop circuit has switching field effect transistors which are connected between the storage field effect transistors and the pulse generator circuit.

17. The circuit arrangement as claimed in claim 16, comprising a first switching field effect transistor, the gate terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor, at the first source/drain terminal of which the second electrical reference potential can be applied, and the second source/drain terminal of which is coupled to a storage node of the storage field effect transistors.

18. The circuit arrangement as claimed in claim 17, comprising a second switching field effect transistor, the gate terminal of which is coupled to the gate terminal of the complementary bypass field effect transistor, at the first source/drain terminal of which the first electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the first switching field effect transistor.

19. The circuit arrangement as claimed in claim 18, comprising a protective field effect transistor, the gate terminal of which is coupled to the gate terminal of the first switching field effect transistor, the first source/drain terminal of which is coupled to the second source/drain terminal of the first switching field effect transistor and to a source/drain terminal of a storage field effect transistor, and the second source/drain terminal of which is coupled to a source/drain terminal of another storage field effect transistor.

20. The circuit arrangement as claimed in one of claims 14 to 19, comprising a fourth signal path of additional field effect transistors, which has the same circuit as the third signal path formed from the field effect transistors of the flip flop circuit, which additional field effect transistors of the flip flop

circuit are interconnected for storing a complementary storage signal which is complementary to the storage signal.